REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02. Made changes to table I, figure 1, figure 3, and figure 4. Editorial changes throughout.	90-06-28	Monica L. Poelking
B	Changes in accordance with NOR 5962-R083-94.	94-03-24	Michael A. Frye
C	Drawing updated to reflect current requirements. - lgt	01-08-23	Raymond Monnin
D	Redraw. Paragraphs updated to the latest MIL-PRF-38535 requirements. -drw	12-10-11	Charles F. Saffle

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

REV																			
SHEET																			
REV																			
SHEET																			
REV STATUS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D					
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13					

PMIC N/A

PREPARED BY
Rick C. Officer

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Charles E. Besore

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
89-08-04

REVISION LEVEL
D

MICROCIRCUIT, LINEAR, CMOS, 14-BIT ANALOG-TO-DIGITAL CONVERTER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-89674**

SHEET 1 OF 13

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-89674	01	X	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function	INL test
01	5014-S	14-bit CMOS analog-to-digital converter, 14.25 μs	±1.5 LSB
02	5014-T	14-bit CMOS analog-to-digital converter, 14.25 μs	±0.5 LSB

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Q	GDIP1-T40 or CDIP2-T40	40	Dual-in-line
X	CQCC1-N44	44	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/

Positive digital supply voltage range ($+V_D$)	-0.3 V dc to +6.0 V dc 2/
Negative digital supply voltage range ($-V_D$)	+0.3 V dc to -6.0 V dc
Positive analog supply voltage range ($+V_A$)	-0.3 V dc to +6.0 V dc
Negative analog supply voltage range ($-V_A$)	+0.3 V dc to -6.0 V dc
Analog ground (AGND) to digital ground (DGND)	±0.5 V dc
Input current, any pin except supplies	±10 mA 3/
Analog input voltage (AIN and V_{REF} pins)	$-V_A$ - 0.3 V dc to $+V_A$ +0.3 V dc
Digital input voltage range	-0.3 V dc to $+V_D$ +0.3 V dc
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+260°C
Junction temperature (T_J)	+195°C
Power dissipation (P_D):	
Case Q	1500 mW
Case X	1100 mW
Thermal resistance, junction to case (θ_{JC})	See MIL-STD-1835
Thermal resistance, junction to ambient (θ_{JA})	
Case Q	45°C/W
Case X	60°C/W

1/ All voltages referenced to AGND and DGND tied together.
2/ In addition $+V_D$ must not be greater than $+V_A$ + 0.3 V dc.
3/ Transient currents of up to 100 mA will not cause latch-up.

1.4 Recommended operating conditions. 1/

Ambient operating temperature range (T_A)	-55°C to +125°C
Positive digital supply voltage ($+V_D$)	+4.5 V dc to $+V_A$ V dc 2/
Negative digital supply voltage ($-V_D$)	-4.5 V dc to -5.5 V dc
Positive analog supply voltage ($+V_A$)	+4.5 V dc to +5.5 V dc
Negative analog supply voltage ($-V_A$)	-4.5 V dc to -5.5 V dc
Digital ground (DGND)	0 V dc
Analog ground (AGND)	0 V dc
Digital input low voltage (V_{IL})	-0.3 V dc to +0.8 V dc
Digital input high voltage (V_{IH})	+2.0 V dc to $+V_D$
Analog reference input voltage (V_{REF}) range	+4.5 V dc
Analog input voltage range:	
Unipolar mode	AGND to $+V_{REF}$
Bipolar mode	$-V_{REF}$ to $+V_{REF}$

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ All voltages referenced to AGND and DGND tied together.
2/ In addition $+V_D$ must not be greater than $+V_A$ + 0.3 V dc.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Block diagram. The block diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Resolution for which no missing codes is guaranteed	RES	1/	1, 2, 3	All	14		Bits
Integral linearity error	INL	1/, 2/	1, 2, 3	01		±1.5	LSB
				02		±0.5	
Differential linearity error	DNL	1/, 2/	1, 2, 3	All		±0.5	LSB
Full-scale error	FSE	1/, 2/	1, 2, 3	All		±1.0	LSB
Full-scale error drift	$dFSE/d_t$	1/, 2/, 3/, 4/	2, 3	All		±1.0	LSB
Unipolar offset error	VOFF	1/, 2/	1, 2, 3	01		±1.0	LSB
				02		±0.75	
Unipolar offset error drift	$dVOFF/d_t$	1/, 2/, 3/, 4/	2, 3	All		±0.5	LSB
Bipolar offset error	BOFF	1/, 2/	1, 2, 3	01		±1.0	LSB
				02		±0.75	
Bipolar offset error drift	$dBOFF/d_t$	1/, 2/, 3/, 4/	2, 3	All		±1.0	LSB
Bipolar negative full-scale error	BNFSE	1/, 2/	1, 2, 3	01		±1.5	LSB
				02		±1.0	
Bipolar negative full-scale error drift	$dBNFSE/d_t$	1/, 2/, 3/, 4/	2, 3	All		±1.0	LSB
Peak harmonic or spurious noise	S/PN	1 kHz input, full scale amplitude, bipolar mode 1/, 2/	4, 5, 6	01	85		dB
				02	94		
		12 kHz input, full scale amplitude, bipolar mode 1/, 2/		01	80		
				02	84		
Analog input capacitance in fine charge mode	C_{IN}	Unipolar mode, T_A = +25°C 1/, 3/	4	All		375	pF
		Bipolar mode, T_A = +25°C 1/, 3/				220	
Signal to noise ratio	S/(N+D)		4, 5, 6	01	80		dB
				02	82		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Digital input voltage ($\overline{HOLD}$, CLKIN, CAL, $\overline{INTRLV}$, BW, RST, BP/$\overline{UP}$, AO, RD, CS)	V_{IH}	5/, 6/	1, 2, 3	All	2.0		V
	V_{IL}					0.8	
Digital input current	I_{IN}	5/, 6/	1, 2, 3	All		±10	µA
Digital output voltage ($D_0 – D_{15}$, SDATA, SCLK, $\overline{EOC}$, $\overline{EOT}$)	V_{OL}	Logic "0", I_{SINK} = -1.6 mA 5/, 6/	1, 2, 3	All		0.4	V
	V_{OH}	Logic "1", I_{SOURCE} = 100 µA 5/, 6/			$+V_D$ -1.0		
High impedance state output current	I_Z	Pins D_0 to D_{15} only 5/, 6/	1, 2, 3	All		±10	µA
Conversion time	t_C	1/, 6/, 7/	9, 10, 11	All		14.25	µs
Acquisition time	t_{ACQ}	T_A = +25°C 1/, 2/, 3/, 8/	9	All		3.75	µs
Throughput	t_{PUT}	1/, 6/, 7/	9, 10, 11	All	55.6		kHz
Positive analog supply current	$+I_A$	$+V_A$, $+V_D$ = 5.5 V, 6/, 9/ $-V_A$, $-V_D$ = -5.5 V	1, 2, 3	All		19.0	mA
Negative analog supply current	$-I_A$	$+V_A$, $+V_D$ = 5.5 V, 6/, 9/ $-V_A$, $-V_D$ = -5.5 V	1, 2, 3	All		19.0	mA
Positive digital supply current	$+I_D$	$+V_A$, $+V_D$ = +5.5 V, 6/, 9/ $-V_A$, $-V_D$ = -5.5 V	1, 2, 3	All		6.0	mA
Negative digital supply current	$-I_D$	$+V_A$, $+V_D$ = +5.5 V, 6/, 9/ $-V_A$, $-V_D$ = -5.5 V	1, 2, 3	All		6.0	mA
Master clock frequency 10/	f_{CLK}	T_A = -55°C, Internally generated CLKIN = 0 V dc, $+V_D$, $+V_A$ = +4.5 V, $-V_D$, $-V_A$ = -4.5 V	11	All	1.75		MHz
$\overline{HOLD}$ pulse width	t_{HPW}	See figure 4 5/, 6/, 11/	9, 10, 11	All	$1/f_{CLK}$ +50	t_C	ns
Data delay time	t_{DD}	See figure 4 5/, 6/, 11/	9, 10, 11	All		100	ns
$\overline{EOC}$ pulse width	t_{EPW}	See figure 4 5/, 6/, 11/	9, 10, 11	All	$4/f_{CLK}$ -20		ns
CAL, $\overline{INTRLV}$ to $\overline{CS}$ low setup time	t_{CS}	See figure 5 5/, 6/, 11/	9, 10, 11	All	20		ns

See footnotes at end of table

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
A0 to $\overline{CS}$ and $\overline{RD}$ low setup time	t_{AS}	See figure 5 5/, 6/, 11/	9, 10, 11	All	20		ns
$\overline{CS}$ or $\overline{RD}$ High to A0 invalid hold time	t_{AH}	See figure 5 5/, 6/, 11/	9, 10, 11	All	50		ns
$\overline{CS}$ High to CAL, $\overline{INTRLV}$ invalid hold time	t_{CH}	See figure 5 5/, 6/, 11/	9, 10, 11	All	50		ns
$\overline{CS}$ low to data valid access time	t_{CA}	$\overline{RD}$ = logic "0", see figure 5 5/, 6/, 11/	9, 10, 11	All		150	ns
$\overline{RD}$ low to data valid access time	t_{RA}	$\overline{CS}$ = logic "0", see figure 5 5/, 6/, 11/	9, 10, 11	All		150	ns
Output float delay	t_{FD}	See figure 5 5/, 6/, 11/	9, 10, 11	All		140	ns
SDATA to SCLK rising setup time	t_{SS}	See figure 6 5/, 6/, 11/	9, 10, 11	All	$2/f_{CLK}$ -50		ns
SCLK rising to SDATA hold time	t_{SH}	See figure 6 5/, 6/, 11/	9, 10, 11	All	$2/f_{CLK}$ -100		ns

1/ $+V_A$, $+V_D$ = +5.0 V; $-V_A$, $-V_D$ = - 5.0 V; V_{REF} = +4.5 V dc; f_{CLK} = 4 MHz; analog source impedance = 200Ω; error tests are done after calibration at the temperature of interest.

2/ Synchronous sampling mode ($\overline{EOT}$ connected to $\overline{HOLD}$), interleave disabled.

3/ This parameter shall be measured only for initial characterization and after process or design changes which may affect this parameter.

4/ Total drift over -55°C to +125°C since calibration at power-up at +25°C.

5/ $+V_A$, $+V_D$ = +5.0 V dc ±10%; $-V_A$, $-V_D$ = -5.0 V dc ±10%.

6/ This parameter is guaranteed, if not tested, at T_A = +25°C. This parameter is tested at T_A = -55°C and +125°C.

7/ Measured from falling transition on $\overline{HOLD}$ to falling transition on $\overline{EOC}$.

8/ Acquisition time is the time allowed by the converter for acquisition of the input voltage prior to conversion.

9/ All outputs unloaded; All inputs swinging between $-V_D$ and 0 V dc.

10/ Externally supplied maximum clock frequency is 4 MHz. Analog parametric measurements are done with the maximum external clock (see footnote 1/).

11/ Inputs: logic "0" = 0 V, logic "1" = $+V_0$; C_L = 50 pF.

Device types	01 and 02	
Case outlines	Q	X
Terminal number	Terminal symbol	
1	$\overline{HOLD}$	$\overline{HOLD}$
2	D_0	D_0
3	D_1	D_1
4	D_2	D_2
5	D_3	D_3
6	D_4	D_4
7	D_5	D_5
8	D_6	D_6
9	D_7	NC
10	DGND	D_7
11	$+V_D$	DGND
12	D_8	$+V_D$
13	D_9	NC
14	D_{10}	D_8
15	D_{11}	NC
16	D_{12}	D_9
17	D_{13}	D_{10}
18	D_{14}	D_{11}
19	D_{15}	D_{12}
20	CLKIN	D_{13}
21	$\overline{CS}$	D_{14}
22	$\overline{RD}$	D_{15}
23	A0	CLKIN
24	$BP/\overline{UP}$	$\overline{CS}$
25	$+V_A$	$\overline{RD}$
26	AIN	A0
27	AGND	$BP/\overline{UP}$
28	V_{REF}	$+V_A$
29	REFBUF	AIN
30	$-V_A$	AGND
31	TST	V_{REF}
32	RST	REFBUF
33	BW	NC
34	$\overline{INTRLV}$	$-V_A$
35	CAL	TST
36	$-V_D$	RST
37	$\overline{EOT}$	BW
38	$\overline{EOC}$	$\overline{INTRLV}$
39	SCLK	CAL
40	SDATA	$-V_D$
41	----	$\overline{EOT}$
42	----	$\overline{EOC}$
43	----	SCLK
44	----	SDATA

NC = Not connected

FIGURE 1. Terminal connections.

Function	$\overline{HOLD}$	$\overline{CS}$	CAL	$\overline{INTRLV}$	$\overline{RD}$	A0	RST
Hold and start convert		X	X	X	X	See note	0
Initiate burst calibration	X	0	1	X	X	See note	0
Stop burst cal and begin track	1	0	0	X	X	See note	0
Initiate interleave calibration	X	0	X	0	X	See note	0
Terminate interleave cal	X	0	X	1	X	See note	0
Read output data	X	0	X	X	0	1	0
Read status register	1	0	X	X	0	0	0
High impedance data bus	X	1	X	X	X	See note	X
High impedance data bus	X	X	X	X	1	See note	X
Reset	X	X	X	X	X	X	1
Reset	0	0	X	X	X	0	X

Note: The status of A0 is not critical to the operation specified. However A0 should not be low with $\overline{CS}$ and $\overline{HOLD}$ low, or a software reset will result.

FIGURE 2. Truth table.

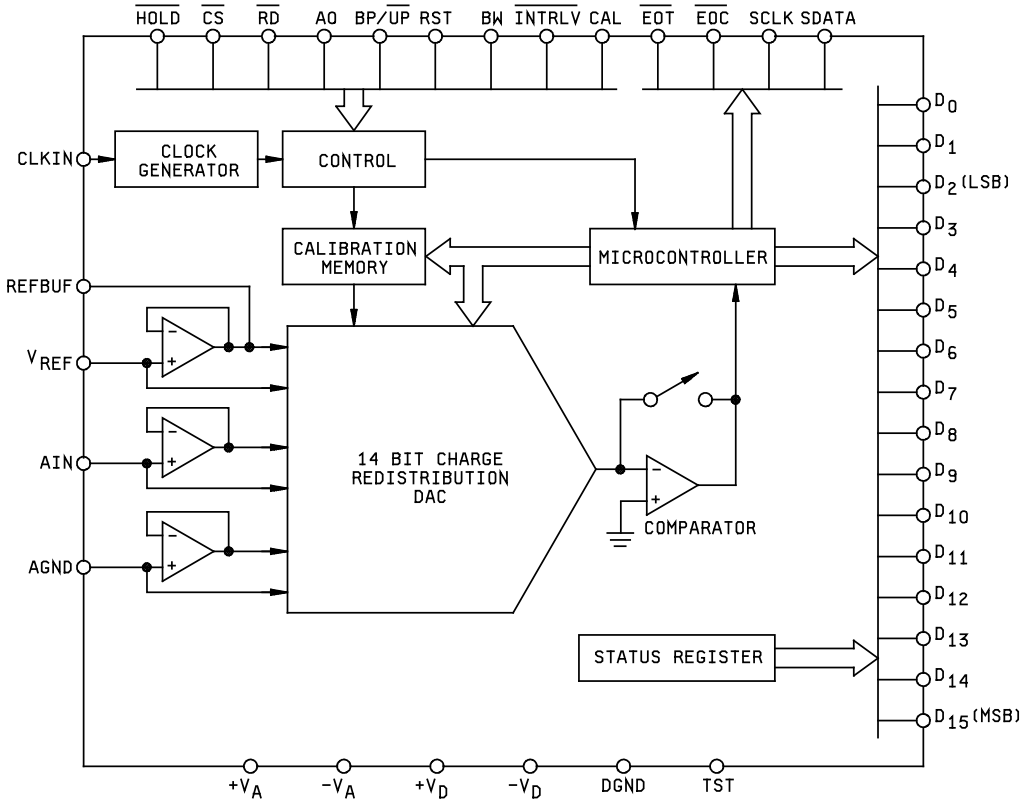

FIGURE 3. Block diagram.

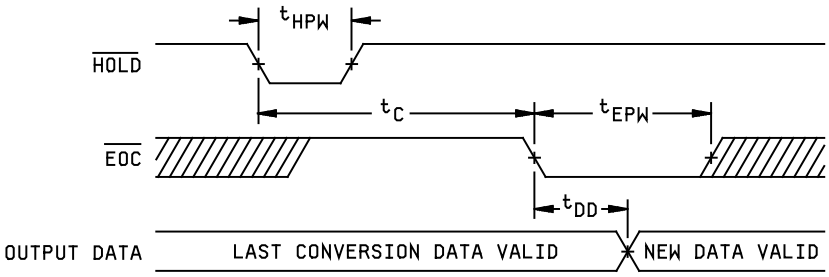

FIGURE 4. Conversion timing.

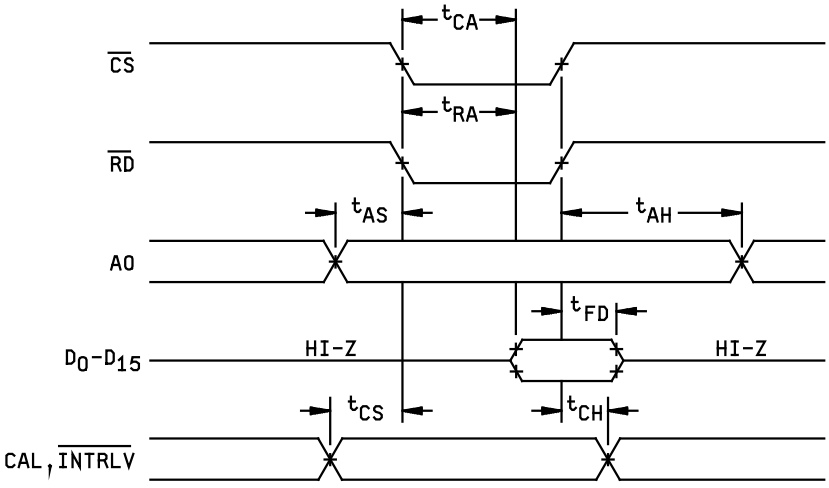

FIGURE 5. Read and calibration control timing.

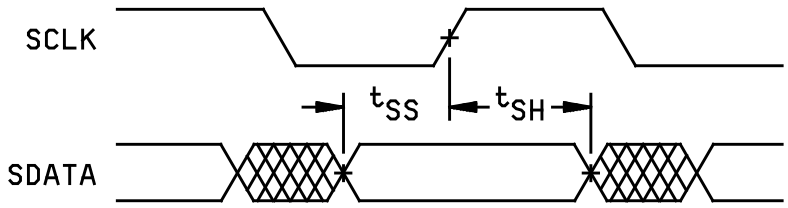

FIGURE 6. Serial output timing.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1, 4
Final electrical test parameters (method 5004)	1*, 2, 3, 4, 5, 6, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 5, 6, 9**, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3

* PDA applies to subgroup 1.
** Subgroup 9 is guaranteed if not tested.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 12-10-11

Approved sources of supply for SMD 5962-89674 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8967401QC	3RNH0	5014-SD14B
	3/	SEI5014-SD14B
	3/	CS5014-SD14B
5962-8967401XC	3RNH0	5014-SE14B
	3/	SEI5014-SE14B
	3/	CS5014-SE14B
5962-8967402QC	3RNH0	5014-TD14B
	3/	SEI5014-TD14B
	3/	CS5014-TD14B
5962-8967402XC	3RNH0	5014-TE14B
	3/	SEI5014-TE14B
	3/	CS5014-TE14B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
3RNH0	XTREME Semiconductor 2801 Oakmont Drive, Bldg. A, Suite 700 Round Rock, TX 78664